

REMARKS

Responsive to the Official Action mailed June 24, 2005, Applicant provides the following remarks. Reconsideration and allowance of the subject application, as amended, are respectfully requested. Claim 7 has been amended to correct a minor typographical error.

Drawings

The Examiner objected to the drawings because reference numeral 218 utilized in FIG. 3 was not mentioned in the description. The Examiner indicated corrected drawings or an amendment to the specification to add the reference numeral in the description was required to avoid abandonment of the application. The Applicant has amended the specification to include the reference numeral 218 as indicated as earlier indicated. Therefore, Applicant respectfully requests the Examiner's objection to the drawings has been overcome.

Double Patenting Rejection

Claims 12 - 17 were provisionally rejected under the judicially created doctrine of double patenting over claims 1 - 6 of copending Application No. 10/442,829 in view of Kobayashi (U.S. Patent No. 6,373,346) and Larson (U.S. Patent No. 5,767,704). In view of the comments and amendments herein, it is respectfully submitted that all of the outstanding rejections are resolved, and therefore the provisional double patenting rejection is the only rejection remaining in the instant application. Accordingly, it is respectfully requested that the provisional double patenting rejection of claims 12 -17 be withdrawn and the instant application allowed to issue. See MPEP §804 I. B.

35 USC §103 Rejection of the Claims

Claims 1 – 3 and 7 - 8

Claims 1 - 3 and 7 - 8 were rejected under 35 USC § 103(a) as being unpatentable over Kobayashi (U.S. Patent No. 6,373,346, hereinafter "Kobayashi") in view of Larson (U.S. Patent No. 5,767,704, hereinafter "Larson"). The Examiner argues that Kobayashi discloses those

elements of Applicant's claim 1 including a duty cycle control circuit to control the duty cycle of the pulse data output signal. The Examiner admits, and Applicant's agree, that Kobayashi does not teach the "duty cycle to be based on an average power of the pulse data output signal." Official Action dated June 24, 2005, page 3, ¶ 3. Rather, the Examiner relies on Larson to provide this missing teaching and argues it would have been obvious to combine the laser driver circuit of Kobayashi with the teachings of Larson. Applicant respectfully traverses this rejection.

Claim 1 is directed to a laser driver circuit requiring "an input stage to receive an input signal; a limiting amplifier to generate a pulse data output signal in response to the input signal, the pulse data output signal comprising a duty cycle; an output stage to modulate an output current signal based upon the pulse data output signal; and a duty cycle control circuit to control the duty cycle of the pulse data output signal based, at least in part, on an approximation of an average power of the pulse data output signal." (emphasis added).

For example, Applicant's FIG. 4 illustrates a laser driver circuit 300 including a duty cycle control circuit 306 and an output stage 310. Applicant's FIG. 5 also further illustrates an embodiment of a duty cycle control circuit 400 providing a pulse data output signal at terminals 414. The duty cycle control circuit 400 controls "the duty cycle of the pulse data output signal, based at least in part, on an approximation of an average power of the pulse data output signal" as required by claim 1.

Kobayashi teaches a laser driver circuit that may provide positive peak control or pre-emphasis (provided by circuit 102 of FIG. 2 or circuit 102' of FIG. 6) and negative peak control or de-emphasis (provided by circuit 104 of FIG. 2 or circuit 104' of FIG. 6). Column 4, lines 19 – 21. The current source I_{CS1} of circuit 102, 102' may provide a weighing factor for the degree of pre-emphasis such that when "the current source $I_{CS1}=0$, zero pre-emphasis will be implemented. When the current source I_{CS1} increases, an increasing degree of pre-emphasis will occur." Column 4, lines 38 – 42. Similarly, the current source I_{CS2} of circuit 104, 104' may provide a weighing factor for the degree of de-emphasis such that when "the current source $I_{CS2}=0$, zero de-emphasis will occur. When the current source I_{CS2} is increased, an increasing degree of de-emphasis will occur." Column 5, lines 1 – 3.

The pre-emphasis and de-emphasis may introduce duty cycle distortion seen in Kobayashi's FIGs. 4a and 5a when compared to FIG. 3a. Column 6, lines 42 – 44. Therefore, in

the embodiment of FIG. 6, Kobayashi teaches a control circuit 150 “implemented as a duty cycle distortion (DCD) control circuit that compensates for the DC offset that may be introduced by the pre-emphasis and de-emphasis circuits 102 and 104.” (emphasis added). Column 6, lines 60 – 63. The duty cycle distortion control circuit may have the current source I_{DCD} of a set or tuned magnitude to “compensate for the output DC offset produced by the pre-emphasis and de-emphasis circuits 102' and 104'.” Column 7, lines 6 – 8. In other words, Kobayashi teaches the duty cycle control circuit 150 is provided to compensate for the amount of DC offset that may be introduced by the pre-emphasis and de-emphasis circuits 102' and 104'.

So not only does Kobayashi not disclose, teach, or suggest “a duty cycle control circuit to control the duty cycle of the pulse data output signal based, at least in part, on an approximation of an average power of the pulse data output signal” as required by claim 1, it actually teaches away from such a limitation by teaching a duty cycle compensation circuit 150 that is provided to compensate for DC offset produced by the pre-emphasis and de-emphasis circuits 102' and 104'. Nowhere does Kobayashi mention “an approximation of an average power of the pulse data output signal” as required by claim 1.

Larson does not provide the missing teachings of Kobayashi. Larson does not disclose, teach, or suggest “a duty cycle control circuit to control the duty cycle of the pulse data output signal based, at least in part, on an approximation of an average power of the pulse data output signal” as required by claim 1.

Larson teaches an “apparatus for supplying current to a laser diode.” Column 1, lines 10 – 11. In Larson’s system of FIG. 1, “the laser diode 4 provides the necessary light in order to read from an electro-optic memory or write upon it.” Column 2, lines 55 – 57. Before a read or a write function, a threshold current is drawn through the laser diode 4 by the threshold current source 14 to bring the laser up to the lasing point. For a read function, a combination of current from the threshold current source 14 and the read current source 12 via the read switch 10 is drawn through the laser diode 4. For a write function, a combination of current from the threshold current source 14 and the write current source 16 via the write switch 18 is drawn through the laser diode 4.

Larson’s FIG. 2 provides details on the read switch 10 of FIG. 1. The read switch 10 includes transistors 20 and 22. In operation, “one transistor is turned on while the other is turned

off.” Column 4, lines 11 – 12. Schottky diodes 24 and 26 are placed in series with the emitters of the differential pair formed by transistors 20 and 22. “The Schottky diodes block the path back through the off transistor and allow only the current source current to be switched, as the path back through the off-transistor is blocked.” Column 4, lines 49 – 53.

Regarding the resistor 28 and capacitor 34 of FIG. 2, Larson teaches:

The resistor 28 and capacitor 34 connected between the cathodes of the Schottky diodes and the current source provide two functions. First, they provide a long term balancing effect due to the time constant (RC) being relatively long (compared to the 300 MHz switching rate). This is needed because the current source is controlled by current in the laser diode and this current only passes through Q1. Thus there is a possibility that the current through Q1 could become significantly less than the current through Q2 and the closed loop control would not know the difference since laser diode power was correct. However, for this to occur, the voltage drop across Q2 base to emitter and the Schottky diode on the Q2 side would be greater than the corresponding voltage drops on Q1's side of the differential switch. The capacitor acts to integrate (average) the voltage at the Schottky diode's cathode and thus prevent the pulse to pulse voltage variations from occurring. Column 6, lines 12 – 28.

In other words, the capacitor 34 helps to prevent pulse to pulse voltage variations that may occur if the current through transistor Q1 was less than the current though transistor Q2. Accordingly, Larson does not disclose, teach, or suggest “a duty cycle control circuit to control the duty cycle of the pulse data output signal based, at least in part, on an approximation of an average power of the pulse data output signal” as required by claim 1

In addition, even assuming *arguendo* that Larson does teach the missing element of Kobayashi, the proposed modification to Kobayashi would render Kobayashi unsatisfactory for its intended purpose. As the Examiner can appreciate, if Kobayashi were to be modified by Larson, the duty cycle compensation circuit 150 would cease to function as intended by Kobayashi. If the proposed modification would render the prior art unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the combined reference. See MPEP §2143.01 and *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). The duty cycle distortion circuit 150 taught by Kobayashi is for compensating for a DC offset introduced by the pre-emphasis and de-emphasis circuits 102' and 104'. If the duty cycle distortion circuit 150 were to control a duty cycle “based on, at least in part, on an approximation of an average

power of the pulse data output signal” it would render Kobayashi unsatisfactory for intended purpose.

In summary, neither Kobayashi nor Larson, alone or in combination, teach “a duty cycle control circuit to control the duty cycle of the pulse data output signal based, at least in part, on an approximation of an average power of the pulse data output signal” as required by claim 1. In addition, even assuming *arguendo* that Larson does teach the missing element of Kobayashi, the proposed modification to Kobayashi would render Kobayashi unsatisfactory for its intended purpose so there is no suggestion or motivation to make the combined reference. Accordingly, Applicant respectfully requests claim 1 is allowable.

Claims 2 - 3 depend from claim 1. Therefore, Applicant respectfully submits claims 2 - 3 are also allowable by virtue of their dependency from claim 1 in addition to their own further limitations.

Claim 7 is an independent claim directed to a method comprising “controlling the duty cycle of the pulse data output signal based, at least in part, upon an approximation of the average power of the pulse data output signal.” For similar reasons adduced above regarding independent claim 1, Applicant respectfully submits claim 7 is also allowable.

Claim 8 depends from claim 7. Therefore, Applicant respectfully submits claim 8 is also allowable by virtue of its dependency from claim 7 in addition to its own further limitations.

Claims 4 – 6 and 9 - 11

Claims 4 - 6 and 9 - 11 were rejected under 35 USC § 103(a) as being unpatentable over Kobayashi in view of Larson and further in view of Gilliland et al. (U.S. Patent No. 6,711,189). Applicant respectfully traverses this rejection. Claims 4 – 6 depend, directly or indirectly, from claim 1 and hence incorporate all the limitations of claim 1. Claims 9 – 11 depend, directly or indirectly from claim 7, and hence incorporate all the limitations of claim 7. Applicant respectfully submits claims 4 – 6 are allowable by virtue of their dependency from claim 1 in addition to their own further limitation, and claims 9 – 11 are allowable by virtue of their dependency from claim 7 in addition to their own further limitations.

Claim 12

Claim 12 was rejected under 35 USC § 103(a) as being unpatentable over Kobayashi in view of Larson and further in view of Kenny (U.S. Patent No. 6,654,565, hereinafter “Kenny”). The Examiner argues that Kobayashi and Larson teach the laser driver outlined in the rejection of claim 1. The Examiner indicates Kobayashi and Larson do not teach the laser driver to be used with a serializer. The Examiner relies on Kenny to supply the serializer teaching.

Applicant respectfully traverses this rejection.

Claim 12 is an independent claim directed to a system requiring a laser driver circuit. The laser driver circuit requires “an input stage to receive an input signal; a limiting amplifier to generate a pulse data output signal in response to the input signal, the pulse data output signal comprising a duty cycle; an output stage to modulate the current signal based upon the pulse data output signal; and a duty cycle adjustment circuit to adjust the duty cycle of the pulse data output signal based, at least in part, on an approximation of an average power of the pulse data output signal.” (emphasis added). For similar reasons above adduced regarding independent claim 1, Applicant respectfully submits claim 12 is also allowable.

Claims 13 - 17

Claims 13 - 17 were rejected under 35 USC § 103(a) as being unpatentable over Kobayashi in view of Larson and Kenny and further in view of Diaz et al. (U.S. Patent No. 6,822,987). Applicant respectfully traverses this rejection. Claims 13-17 depend, directly or indirectly, from claim 12 and hence incorporate all the limitations of claim 12. Applicant respectfully submits claims 13 - 17 are allowable by virtue of their dependency from claim 12 in addition to their own further limitations.

Conclusion

Having dealt with all the objections raised by the Examiner, it is respectfully submitted that the present application, as amended, is in condition for allowance. Thus, early allowance is earnestly solicited.

If the Examiner desires personal contact for further disposition of this case, the Examiner is invited to call the undersigned Attorney at 603-668-6560.

In the event there are any fees due, please charge them to our Deposit Account No. 50-2121.

Respectfully submitted,

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Date 9-26-05

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 26 day of September, 2005.

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Signature

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